



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

BS

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,113	03/26/2004	Colin Scott Ramsay	W0583.70014 US00	9227
23628	7590	03/30/2007	EXAMINER	
WOLF GREENFIELD & SACKS, P.C. 600 ATLANTIC AVENUE BOSTON, MA 02210-2206			PEIKARI, BEHZAD	
		ART UNIT		PAPER NUMBER
				2189

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/811,113	RAMSAY ET AL.	
	Examiner B. James Peikari	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 12/18/06.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-26 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 26 March 2004 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____ .

## DETAILED ACTION

### ***Election/Restrictions***

1. Newly submitted claims 27-38 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the features of at least claims 27, 32 and 36 have not been presented before and thus have not been considered by the examiner. Claims 27-38 would require further consideration and searches that were not required for claims 1-26.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 27-38 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### ***Drawings***

2. The drawings are objected to because:

- (A) the view numbers are not in accordance with 37 CFR 1.84(u)(1). For example, "FIG. 1" should replace "Fig. 1", "FIG. 2" should replace "Fig. 2", etc.; and
- (B) the empty boxes in Figures 1 and 6 should be properly labelled.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement

drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency.

Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

3. The specification is objected to because the title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
  
4. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 3-5, 7, 10-14, 20-22, and 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Brown et al. (US Patent 6,879,139 B2), hereinafter simply Brown.

Regarding claim 1, Brown teaches a controller comprising:

a logic core having a plurality of inputs and a plurality of outputs (Fig. 1,

PRIMARY CONTROL UNIT 11 and SECONDARY CONTROL UNIT 12; column 4, lines 24-67); and

a memory (column 2, lines 55-58);

wherein the controller functions as a state machine and upon the transition from a state to a succeeding state the operation of the logic core (column 5, lines 13-24) is modified in accordance with data held in the memory (column 3, lines 60-67; column 5, lines 54-67).

Regarding claim 3, Brown teaches a controller, in which the logic core includes a fault detector (column 3, lines 41-52).

Regarding claim 11, Brown teaches a controller in which the logic core comprises a sequence detector (column 3, lines 41-52).

Regarding claims 4 and 12, Brown teaches a controller, in which the fault detector has a plurality of inputs and a lesser number of outputs (column 4, lines 38-52).

Regarding claims 5 and 13, Brown teaches a controller, in which the fault detector has a single output (column 2, lines 27-34).

Regarding claim 7, Brown teaches a controller, in which at least one input detector has multiple signal inputs (column 4, lines 24-67) and it is responsive to the order in which the signal inputs change (column 1, lines 46-57).

Regarding claim 10, Brown teaches a controller, in which the logic core includes a combinational logic unit having a plurality on inputs and a single output, and wherein at least one of the inputs is selectively maskable and invertable such that the combinational logic unit can be arranged to look for the occurrence of a plurality of input signals being in a predetermined state, and to assert a first predetermined output signal when the input signals are in the predetermined state and a second

predetermined output signal when the input signals are not in the predetermined state (column 2, lines 35-50).

Regarding claim 14, Brown teaches a controller, in which the sequence detector comprises a multiplexer responsive to a selection control word to select only one of the plurality of inputs (column 12, lines 5-9).

Regarding claims 20 and 21, Brown teaches a controller in which the memory is user programmable (column 3, lines 53-67).

Regarding claim 22, Brown teaches a controller, in which the memory is non-volatile (column 2, lines 55-58).

Regarding claim 25, Brown teaches a power supply controller (column 3, lines 53-59).

Regarding claim 26, Brown teaches an integrated circuit including a controller (column 5, lines 10-13).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 2, 6, 9, 8, 15-19 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. (US Patent 6,879,139 B2), hereinafter simply Brown, in view of MacSorley et al. (US Patent 3,626,427), hereinafter simply MacSorley.

Regarding claims 6 and 23, Brown teaches a controller, in which at least one input of the fault detector is associated with a respective input detector which is responsive to at least one of: a mask/select control signal for determining whether an input signal at a signal input of the input detector should be taken into consideration by the fault detector (column 3, lines 53-67).

Brown fails to teach an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal. MacSorley teaches an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal (column 28, lines 35-50; column 48, lines 68-75). At the time of

invention it would have been obvious to a person of ordinary skill in the art to combine the Brown with MacSorley. The motivation for doing so would have been a protection of the storage by storage protection circuitry and address the unreachable portion of storage (column 335, lines 74-75; column 336, lines 1-10).

Regarding claim 2, Brown and MacSorely teach a controller, in which the logic core represents a state having up to three outputs (See Brown, column 4, lines 24-67, it is clear that outputs can be up to three).

Regarding claim 8, Brown and MacSorley teaches a controller, in which the fault detector includes combinational logic for combining its inputs in a logical OR (See MacSorely, column 48, lines 1-10).

Regarding claims 9 and 15, Brown and MacSorely teach a controller, in which an output of the fault detector is supplied to a device arranged in a first mode to pass the output of the fault detector in a non-inverted state (See MacSorely, column 29, lines 60-64) and in a second mode to invert the output of the fault detector (See MacSorely, column 28, lines 35-50; column 48, lines 68-75).

Regarding claims 16 and 17, Brown and MacSorely teach a controller in which the sequence detector further includes a sequence timer arranged to assert an output signal only when an input condition monitored by the sequence detector has been in a

predetermined state for a predetermined period (See MacSorely, column 224, lines 20-26).

Regarding claims 18 and 24, Brown and MacSorely teach a controller as claimed in claim 1, in which the logic core comprises a time out circuit having a time out timer selectively arranged to assert an output a predetermined period after the logic core has entered a state (See MacSorely, column 76, lines 1-8).

Regarding claim 19, Brown and MacSorely teaches a controller, in which the time out timer is programmable (See MacSorely, column 333, lines 25-45).

### ***Response to Arguments***

9. Applicant's arguments filed on December 18, 2006 have been fully considered but they are not persuasive. Applicant's arguments hinge on two features of the claims:

(A) First, applicant states that in Brown, "There is no modification of the logic core upon state transitions". The examiner agrees. However, this statement is not commensurate in scope with the claimed invention. For example, claim 1 states, "upon the transition from a state to a succeeding state the *operation* of the logic core is modified" (emphasis added). That is, the operation of the logic core is changed, but not the core itself. Brown teaches this feature because the logic core operates differently or provides different results, depending on the state of the state machines.

Art Unit: 2189

(B) Second applicant states that "Brown does not really form a single state machine". However, this statement is not commensurate in scope with the claimed invention. There is no requirement for only a single state machine or negative limitation in the claims to exclude other state machines. Even so, applicant has not provided a requisite explanation of why a combination of state machines cannot be considered a state machine. As an analogy, a program comprised on many smaller programs (program modules or subroutines) is still a program.

For at least these reasons, the rejection is maintained.

***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (571) 272-4185. The examiner is generally available between 7:00 am and 7:30 pm, EST, Monday through Wednesday, and between 5:30 am and 4:00 pm on Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon, can be reached at (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center at 866-217-9197 (toll-free).



B. James Peikari  
Primary Examiner  
Art Unit 2189  
3/19/07